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IN THE CLAIMS

Please amend claims 1, 2, 13-16, 18, 19, 23, 28, and 29 as follows:

1. (Currently Amended) A data storage and retrieval system operating on a host computer, the data storage and retrieval system comprising:

a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device, the sparing system comprising computer readable instructions stored in a host memory of the host computer; and

an error correction code system configured to encode data with an error correction code, store the data into the memory device, and decode the encoded data with the error correction code to retrieve the data from the memory device, the error correction code system comprising computer readable instructions stored in the host memory of the host computer.

2. (Currently Amended) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored ~~on~~ in the host ~~computer~~memory.

3. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the memory device.

4. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from a tester that tests the memory device.

5. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from the sparing system that is configured to test the memory device to obtain the entries for the sparing table.

6. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table, and the sparing system and the error correction code system are configured to update the sparing table as defective memory sections are detected in the memory device.

7. (Original) The data storage and retrieval system of claim 1, where the sparing system comprises a sparing table and the error correction code system is configured to detect defective memory sections in the memory device, and the sparing system is configured to update the sparing table with address locations of the detected defective memory sections in the memory device.

8. (Original) The data storage and retrieval system of claim 7, where the error correction code system is configured to correct errors in a selected memory section of the memory device, count the errors to obtain an error count and compare the error count to a threshold value to establish if the selected memory section is defective.

9. (Original) The data storage and retrieval system of claim 8, where the threshold value is greater than 50% of a power of the error correction code.

10. (Original) The data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode all data stored in the memory device.

11. (Original) The data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode selected data stored in the memory device.

12. (Original) The data storage and retrieval system of claim 1, where the error correction code is a Reed-Solomon error correction code.

13. (Currently Amended) A host computer, comprising:

a host memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and

a host processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer.

14. (Currently Amended) The host computer of claim 13, where the host processor executes instructions to replace addresses before the processor executes instructions to encode and decode data with the error correction code during data transfers.

15. (Currently Amended) The host computer of claim 13, where the host processor executes instructions to encode data with the error correction code before the host processor executes instructions to replace addresses during a write operation.

16. (Currently Amended) The host computer of claim 13, where the host processor executes instructions to provide sequential address data transfers between the storage device and the host computer.

17. (Original) The host computer of claim 16, where the sequential address data transfers are divided into sub-transfers around addresses of defective memory sections that are replaced with addresses of spare memory sections.

18. (Currently Amended) The host computer of claim 13, where the host memory stores instructions for a digital camera and the host processor executes the instructions to perform functions of the digital camera.

19. (Currently Amended) The host computer of claim 13, where the host memory stores instructions for a personal digital assistant and the host processor executes the instructions to perform functions of the personal digital assistant.

20. (Original) The host computer of claim 13, where the storage device comprises a magnetic random access memory.

21. (Original) The host computer of claim 13, where the storage device comprises a phase change random access memory.

22. (Original) The host computer of claim 13, where the storage device comprises a probe-based memory.

23. (Currently Amended) A host computer system, comprising:

means for correcting errors in data retrieved from a storage style memory device, the means for correcting errors comprising computer readable instructions stored in a host memory of the host computer system;

means for identifying defective sections of memory in the storage style memory device, where the defective sections of memory provide more errors than a predetermined threshold value; and

means for sparing the defective sections of memory with replacement sections of memory in the storage style memory device, the means for sparing comprising computer readable instructions stored in the host memory of the host computer system.

24. (Original) The computer system of claim 23, where the means for correcting errors comprises a multiple-bit per symbol error correction code.

25. (Original) The computer system of claim 23, where the means for correcting errors comprises a single-bit per symbol error correction code.

26. (Original) The computer system of claim 23, where the means for identifying comprises:

means for counting the number of errors in a selected section of memory in the storage style device;

means for comparing the number of errors to the predetermined threshold value to obtain a compare result; and

means for indicating if the selected section of memory is defective based on the compare result.

27. (Original) The computer system of claim 23, where the means for identifying comprises:

means for storing an address location of one of the defective sections; and

means for storing an address location of one of the replacement sections, where the address location of one of the replacement sections corresponds to the address location of one of the defective sections.

28. (Currently Amended) The computer system of claim 27, where the means for sparing comprises means for replacing the address location of one of the defective sections with the corresponding address location of one of the replacement sections during data transfers between the host computer system and the storage style memory device.

29. (Currently Amended) A ~~computer readable medium having computer executable instructions for performing a~~ method for storing and retrieving data, comprising:

providing a host computer and a memory device;

providing computer-executable sparing instructions and error correction code instructions;

replacing addresses for defective memory sections in a memory device with addresses for replacement memory sections in the memory device by executing the sparing instructions on the host computer;

providing the addresses for the replacement memory sections to the memory device during read and write operations with the memory device by executing the sparing instructions on the host computer;

encoding original data with an error correction code to write encoded data into the memory device by executing the error correction code instructions on the host computer; and

decoding data retrieved from a selected memory section of the memory device with the error correction code by executing the error correction code instructions on the host computer.

30. (Original) The method of claim 29, comprising:

maintaining a table of the addresses for defective memory sections and the addresses for replacement memory sections; and

searching the table to match original addresses with the addresses for defective memory sections.

31. (Original) The method of claim 29, comprising:

updating a table with new addresses for defective memory sections; and

assigning new addresses for replacement memory sections that correspond with the new addresses for defective memory sections.

32. (Original) The method of claim 29, comprising:

counting errors in the data retrieved from the selected memory section to obtain an error count;

comparing the error count to error correction capabilities of the error correction code; and

indicating the selected memory section is defective if the number of errors exceeds a predetermined portion of the error correction capabilities.

33. (Original) A method for storing and retrieving data, comprising:

providing a host computer and a storage style memory device;

providing computer-executable sparing instructions and error correction code instructions;

sparing out sections of memory in the storage style memory device by executing the sparing instructions on the host computer; and

encoding and decoding data stored in the storage style memory device with an error correction code by executing the error correction code instructions on the host computer.

34. (Original) The method of claim 33, comprising:

detecting grown defective sections of memory in the storage style memory device; and

sparing out the detected grown defective sections of memory.

35. (Original) The method of claim 33, comprising:

encoding only selected data; and

decoding only the encoded data stored in the storage style memory device.